

## International conference on semiconductor chip design and manufacturing

Organized by

**School of Engineering, Indrashil University**

### Research Paper Presentation Schedule

22<sup>nd</sup> June 2025, 9:00AM to 10:30AM

| Sr.No. | Research paper Title   | Author  | Affiliation  |
|--------|--|---|--|
| 1.     | Low-Power Smart Grid Management System Using Real-Time Feedback Control  | Mahatta Purohit, Prachi Bhansali, Pragati Shukla, Parth S. Thakar, Amit Kumar | Department of Electronics and Communication Engineering<br>Pandit Deendayal Energy University, Gandhinagar, Gujarat, India   |
| 2.     | Achieving Performance benchmark for Next Gen AI data centre using 5nm devices  | Darshan Bhuva, Vishal Mahida  | eInfochips-An Arrow Company<br>Ahmedabad, India  |
| 3.     | A Hybrid frame work on Attack Mitigation Methodologies in MANETS   | Nidumukkala Bharathi, Parvinder Sing, Vishal Waliya                           | Department of Electronics and Communication Engineering.<br>PhD Scholar<br>Lovely Professional University.<br>Punjab   |
| 4.     | A Review on Changing Trends in Mobile Security using Light Weight Cryptography, AI based Threat Analytics and Decentralized Identity Protocols | Aakanksha Taliwal, Ramji Gupta  | Department of Electronics & Communication Engineering,<br>Parul Institute of Engineering & Technology, Faculty of Engineering & Technology,<br>Parul University, Vadodara, Gujarat |
| 5.     | Green Nano electronics: Role of Recyclable and Low-Carbon Semiconductor Materials in Future Electronics  | Panchal Ketan D. Kumaril Patel<br>Rajendra Patel                              | Department of Mechanical Engg<br>Dr. S. & S.S. Ghandhy Govt. Engg. College Surat, INDIA<br>&<br>Sapphire Software Solution   |
| 6.     | High Isolation SP2T Switch MMIC based 2-channel Ka-band Switch Matrix for Space Applications   | Prolay Verma, Anshul Joshi, Sumit Srivastava, Puja Srivastava, Jayesh Thakkar | Space Applications Centre<br>Indian Space Research Organisation, Department of Space Ahmedabad, India  |
| 7.     | Design of Dual-Port Static Random Access Memory (SRAM) using the RTL to GDS-II Flow in Cadence EDA Tools                                       | Abhishek Jani   | Department of Electrical Engineering Institute of Technology, Ahmedabad, India   |
| 8.     | Comparing the Average Delay and Power Consumption of Decoders Using Pass Transistor, Pseudo-NMOS, and Static CMOS in 45nm Technology           | Ranjitha B T, Dr. Chaitra C   | Dept. of EIE, Siddaganga Institute of Technology Tumkur, Karnataka, INDIA  |

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|----|---|--|--|
| 9. | Contact Engineering in Monolayer WS <sub>2</sub> Transistors: Halogen Doping and Interlayer Strategies for Schottky Barrier Reduction                       | Sharda Devi  | Electrical Engineering, IIT Gandhinagar  |
| 10 | Power-Delay Trade-Offs in Full Adder Designs: A Comparative Study Across Logic Styles and Technologies  | Pallavi Darji, Vala Parth, Arpita Patel, Purvang Dalal | EC Department, Dharamsinh Desai University, Nadiad-387001, Gujarat, India, <sup>2*</sup> EC Department, Charotar University of Science and Technology, Changa, Anand, Gujarat, India |
| 11 | Power Management verification of GNSS Receiver ASIC   | Varenyam   | Space Applications Centre, Ahmedabad, INDIA, (ISRO)  |
| 12 | RTL to GDS-II Design Flow for 8-bit ALU in Cadence Tool   | Patel Krish, Manish Patel                              | Dept. of Electrical Engineering Nirma University Ahmedabad, India  |
| 13 | ComputLitho – An Indigenous OpticalLithography Simulatorwith Novel Features   | Radhika Joglekar                                       | Indian Institute of Technology Gandhinagar   |
| 14 | Design and implementation of an 8-point Fast Fourier Transform (FFT) unit utilizing a Radix-2 algorithm and leveraging the Posit number system architecture | Tanay Shah, Tejas Patel                                | PDEU, Gnadhinagar  |
| 15 | The Design and implementation of a basic 16-bit custom CPU on an FPGA platform, with an emphasis on low-power operation through clock gating                | Gunjan Thakur  |  |
| 16 | A Comprehensive Review of Low-Power High-Speed Multipliers for Error Resilient Applications   | Dr. Swati V. Sakhare                                   | Parul Institute of Engg. & Technology, Parul University, Vadodara  |
| 17 | The Design and implementation of a basic 16-bit CPU, following a structured flow from RTL to GDSII using synopsys tools                                     | Nirbhay Bhojani  | PDEU, Gandhinagar  |